

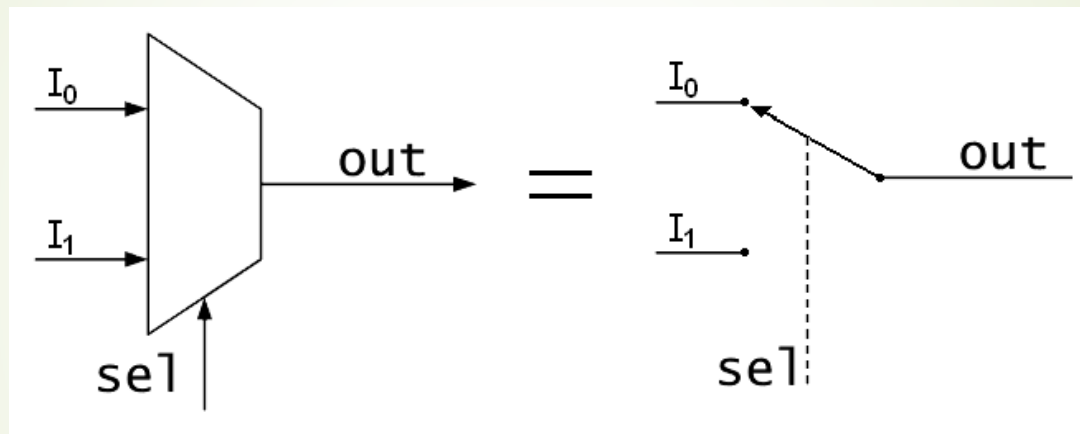
EGC220 Class Notes 3/24/2023

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Division of Engineering Programs

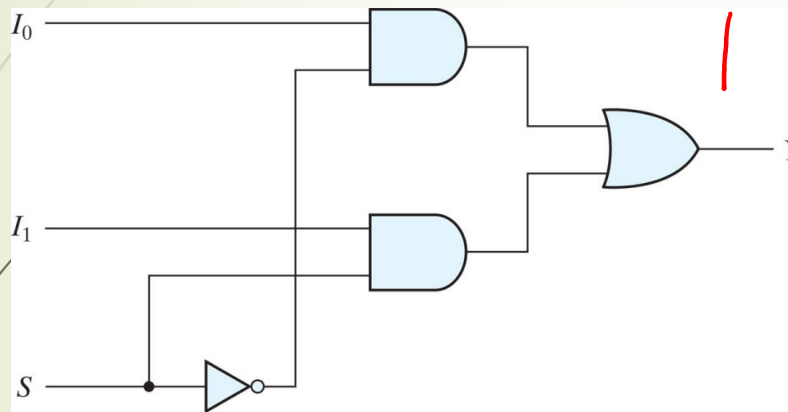
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Two-to-one-line multiplexer

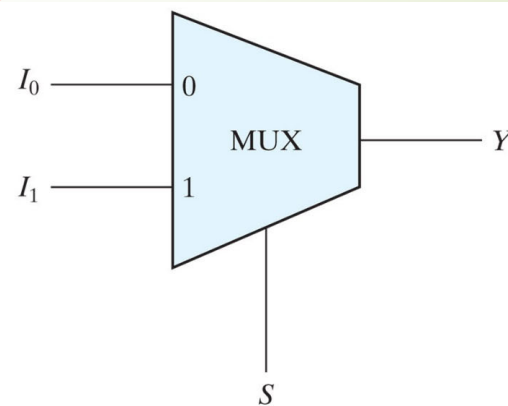


Two-to-one-line multiplexer

$$\begin{array}{c|c} S & Y \\ \hline 0 & I_0 \\ 1 & I_1 \end{array} \quad Y = \bar{S}I_0 + SI_1$$



(a) Logic diagram



(b) Block diagram

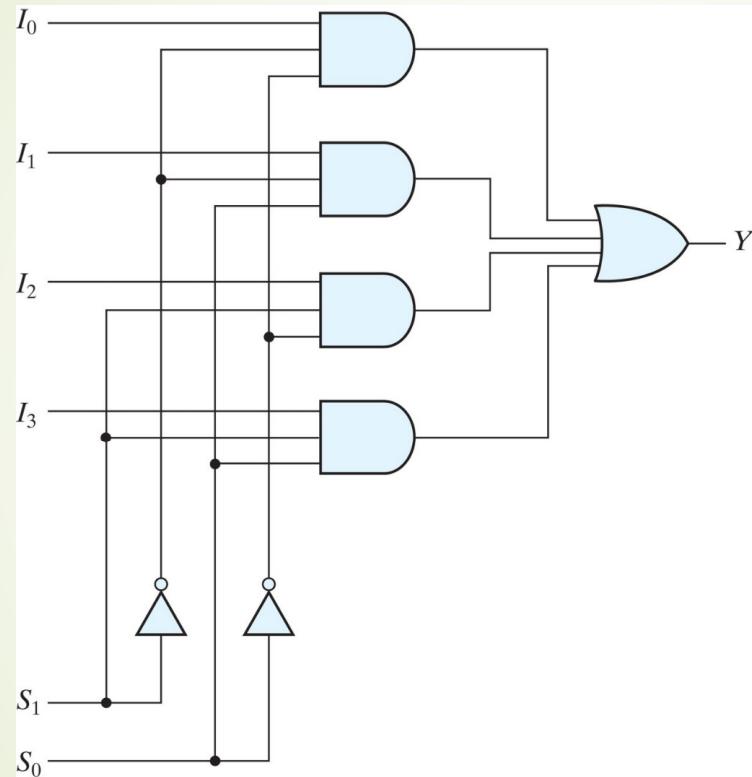
4x1 MUX



S_1	S_0	Z
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Z = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

Four-to-one-line multiplexer



(a) Logic diagram

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(b) Function table

Truth Table of an 8 × 3 Encoder

Table 4.7
Truth Table of an Octal-to-Binary Encoder

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

V
0
1
1

Truth Table of a Priority Encoder

Table 4.8
Truth Table of a Priority Encoder

Inputs				Outputs		
D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Problem 1

Obtain the truth table for an 8×3 priority encoder with inputs $D_0 - D_7$ and output X, Y, Z, V (valid).

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z	V
0	0	0	0	0	0	0	0	X	X	X	0
1	0	0	0	0	0	0	0	0	0	0	1
X	1	0	0	0	0	0	0	0	0	1	1
X	X	1	0	0	0	0	0	0	1	0	1
X	X	X	1	0	0	0	0	0	1	1	1
X	X	X	X	1	0	0	0	1	0	0	1
X	X	X	X	X	1	0	0	1	0	1	1
X	X	X	X	X	X	1	0	1	1	0	1
X	X	X	X	X	X	X	1	1	1	0	1

$$V = \overline{D_7 D_6 D_5 D_4} \overline{D_3 D_2 D_1 D_0}$$

$$V = D_7 + D_6 + D_5 + \dots + D_0$$

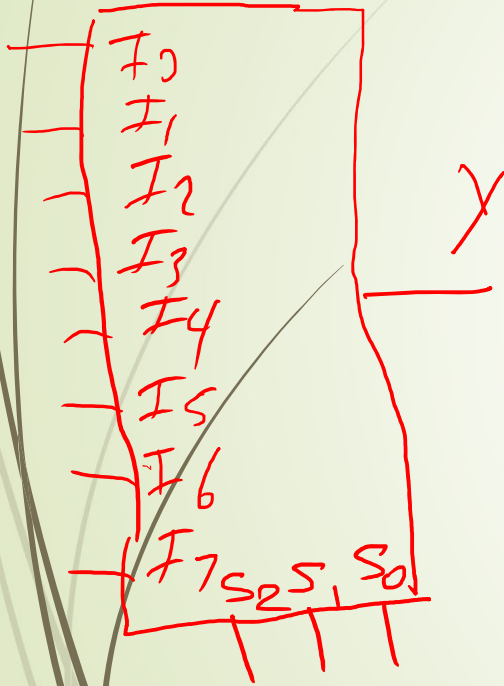
$$X = D_4 + D_5 + D_6 + D_7$$

$$Y = D_2 + D_3 + D_6 + D_7$$

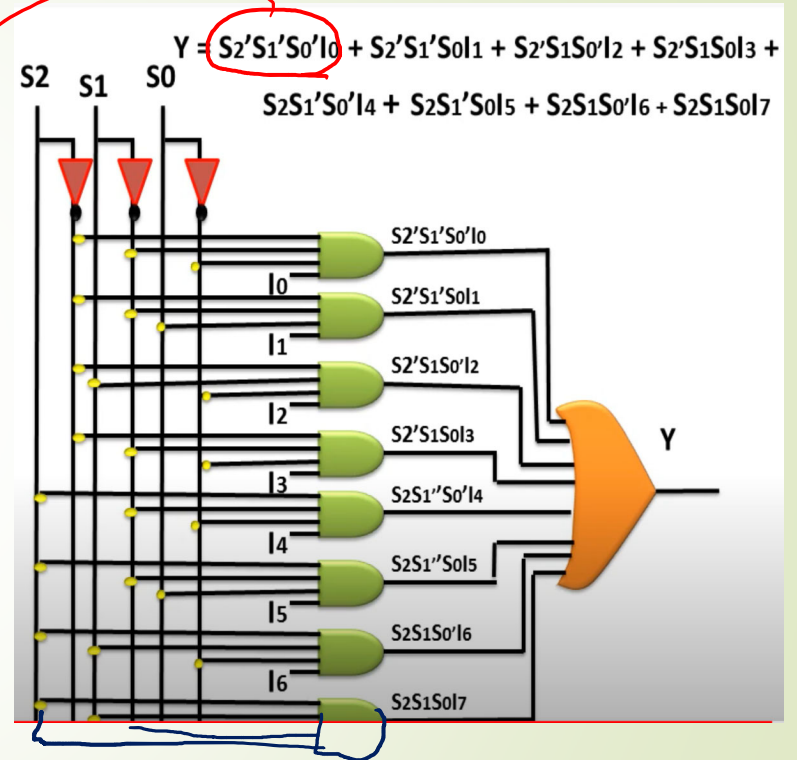
$$Z = D_1 + D_3 + D_5 + D_7$$

Problem 2
Design an 8×1 Mux.

$8 = 2^3 \rightarrow$ select

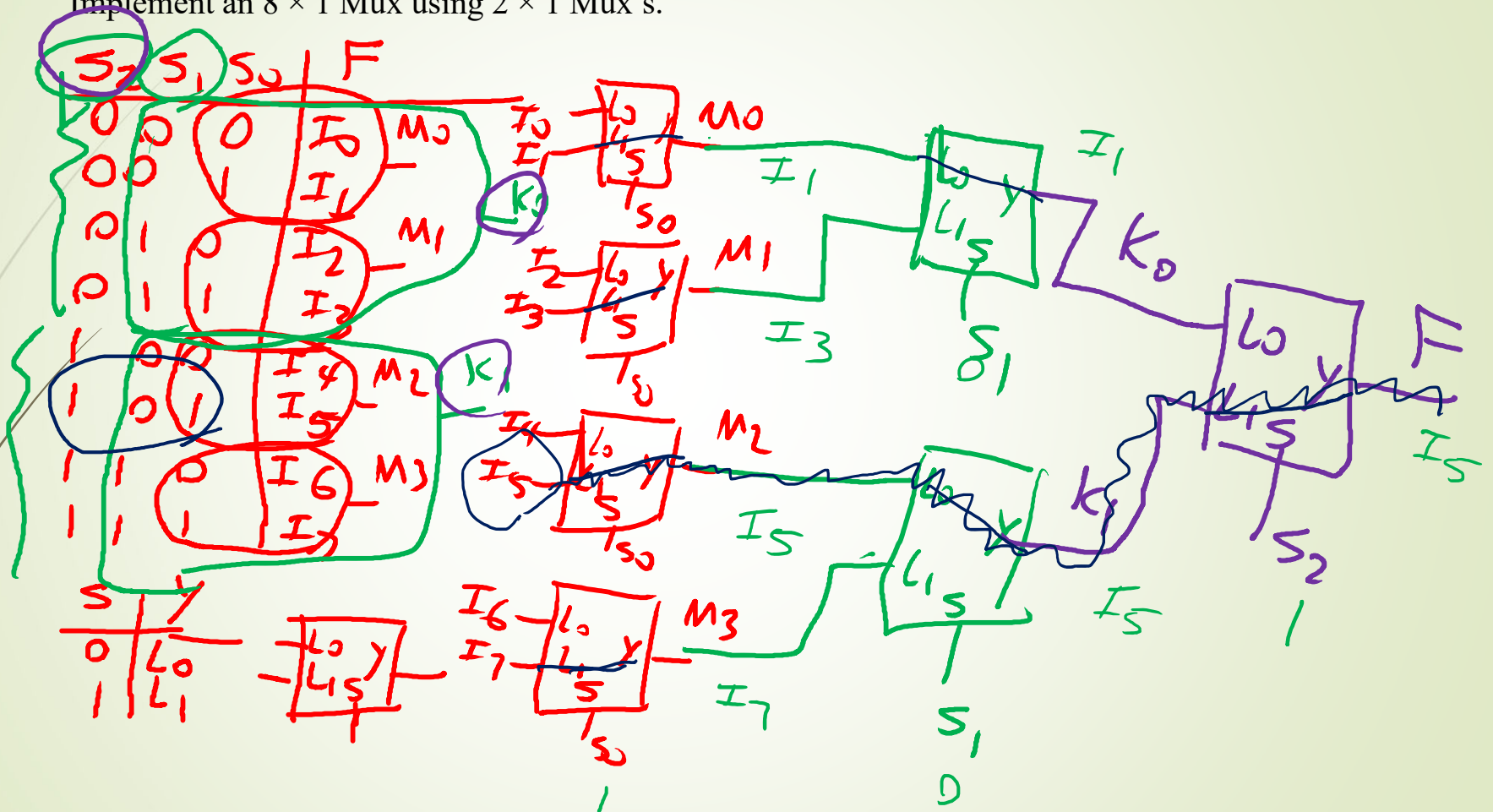


S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7



Problem 3

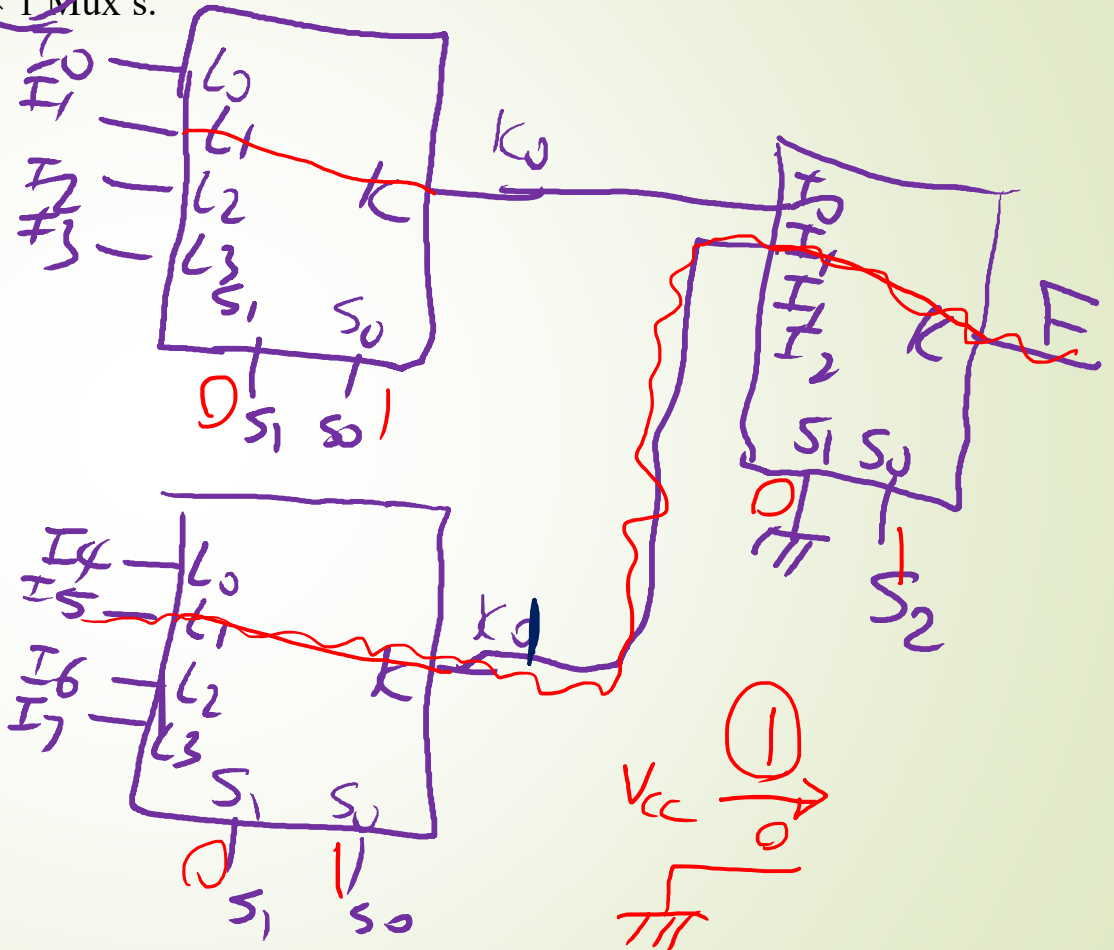
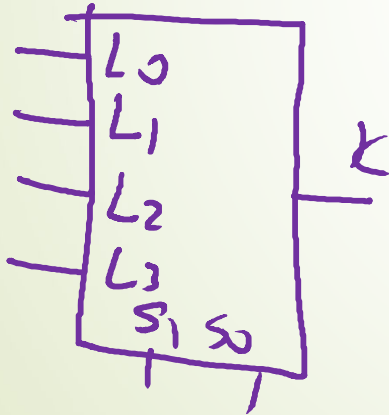
Implement an 8×1 Mux using 2×1 Mux's.



Problem 4

Implement a 16×1 Mux using 4×1 Mux's.

S_1	S_0	K
0	0	L_0
0	1	L_1
1	0	L_2
1	1	L_3

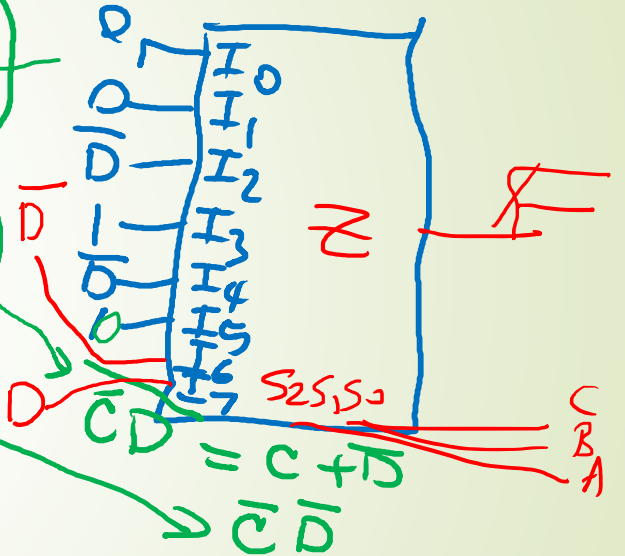
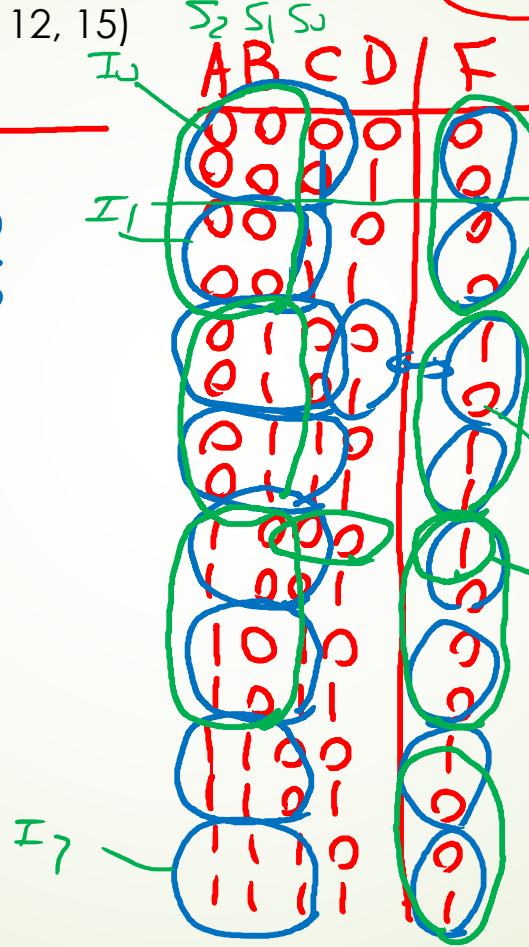


Problem 5

Implement the following Boolean expression using an 8×1 Mux.

$F(A, B, C, D) = \sum m(4, 6, 7, 8, 12, 15)$

A	B	C	Σ
S_2	S_1	S_0	
0	0	0	$I_0 \rightarrow 0$
0	0	1	$I_1 \rightarrow 0$
0	1	0	$I_2 \rightarrow 1$
0	1	1	$I_3 \rightarrow 1$
1	0	0	$I_4 \rightarrow 1$
1	0	1	$I_5 \rightarrow 1$
1	1	0	$I_6 \rightarrow 1$
1	1	1	$I_7 \rightarrow 1$



$\bar{C}\bar{D} + CD = C \oplus D$

Problem 6

Repeat Problem 5 using a 4 × 1 Mux and external gates.

A	B	F
S ₁	S ₀	
00	I ₀	→ 0
01	I ₁	→ C + D
10	I ₂	→ $\overline{C} \overline{D}$
11	I ₃	→ C ⊕ D

C	D	W
00	0	1
01	0	1
10	1	0
11	1	1

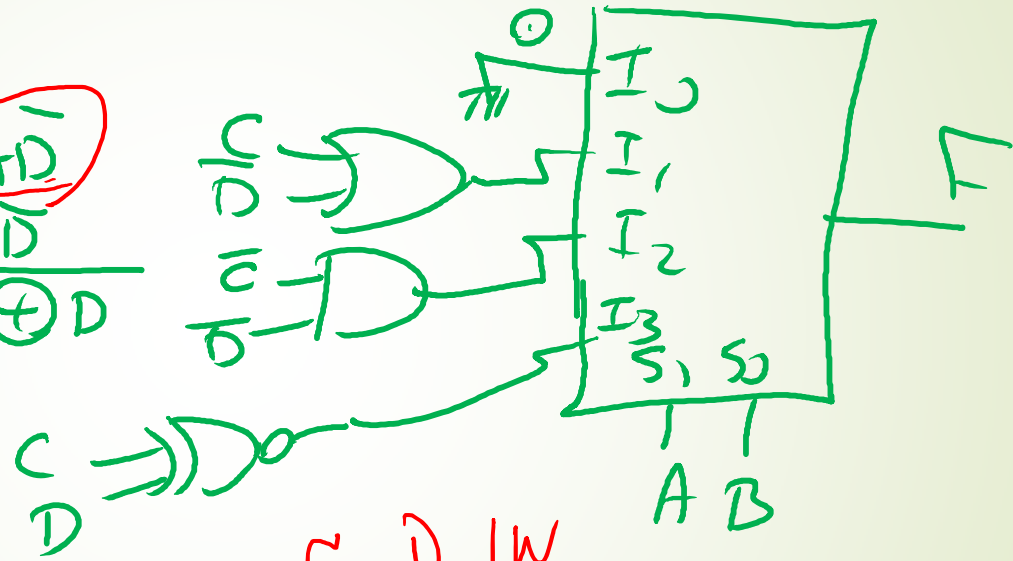
$$W = \overline{C} \overline{D}$$

$$W = C + D$$

C	D	W
00	0	1
01	0	1
10	1	0
11	1	1

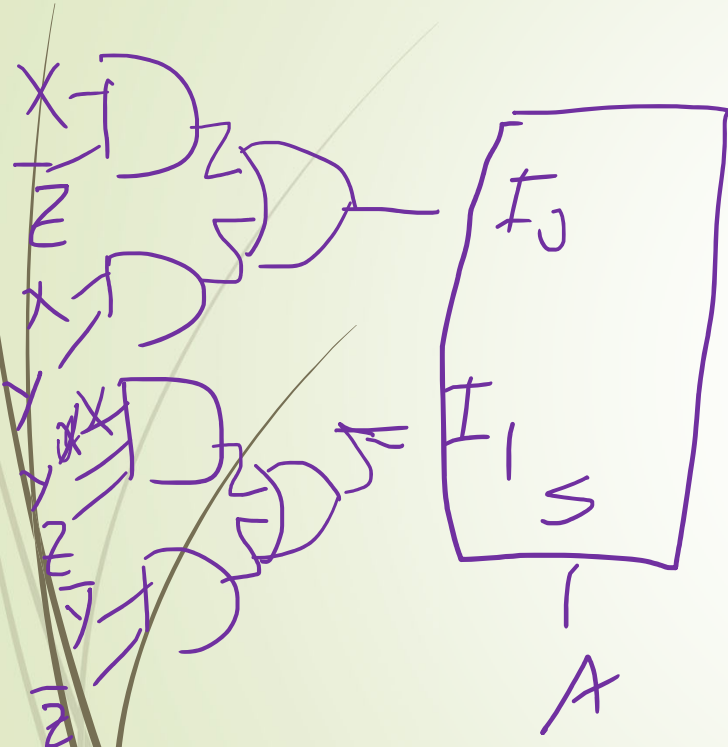
$$W = \overline{C} \overline{D} + (C D)$$

$$= \overline{C \oplus D}$$



Problem 7

Repeat Problem 5 using a 2×1 Mux and external gates.



x	y	z	
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



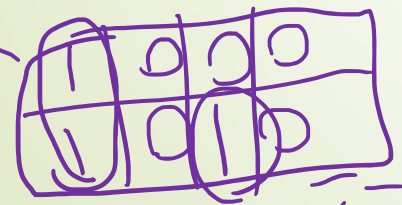
$$X\bar{z} + XY$$

Problem 5

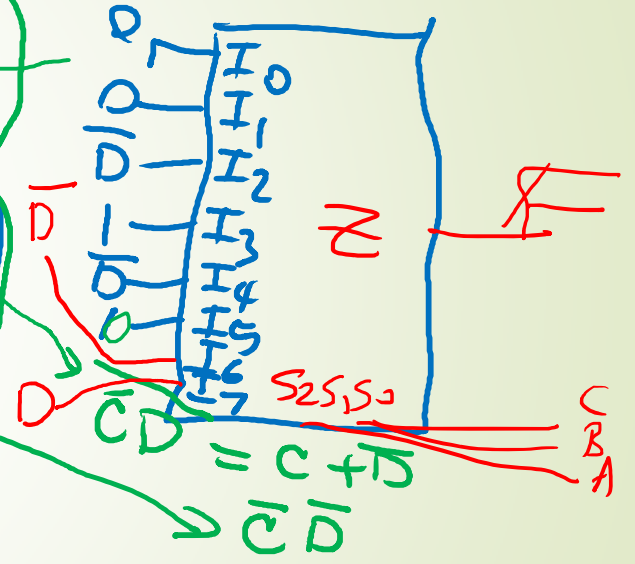
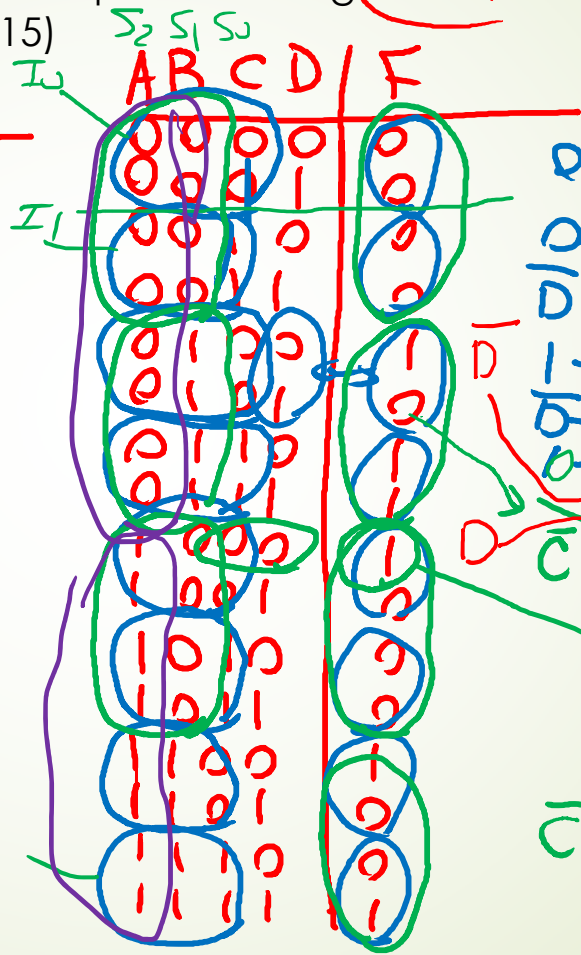
Implement the following Boolean expression using an 8×1 Mux.

$F(A, B, C, D) = \sum m(4, 6, 7, 8, 12, 15)$

A	B	C	\bar{z}
S_2	S_1	S_0	
0	0	0	$I_0 \rightarrow 0$
0	0	1	$I_1 \rightarrow 0$
0	1	0	$I_2 \rightarrow 1$
0	1	1	$I_3 \rightarrow 1$
1	0	0	$I_4 \rightarrow 1$
1	0	1	$I_5 \rightarrow 1$
1	1	0	$I_6 \rightarrow 1$
1	1	1	$I_7 \rightarrow 1$



$\bar{X}\bar{Z} + XY\bar{Z}$



$\bar{C}\bar{D} + CD = \overline{C \oplus D}$